

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

John T. Moore

Serial No.: Not yet assigned

Filed: March 2, 2004

For: TRANSISTOR WITH NITROGEN-HARDENED GATE OXIDE

Examiner: Unknown

Group Art Unit: Unknown

Attorney Docket No.: 2269-4308.4US
(99-1199.04/US)

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INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The present application is a continuation of application Serial No. 10/010,025, filed December 6, 2001, pending, which is a divisional of application Serial No. 09/585,688, filed June 1, 2000, now U.S. Patent No. 6,342,437, issued January 29, 2002

Pursuant to M.P.E.P. 2001.06(b), the Examiner is respectfully requested to consider the information of record in the prior application, and to confirm in the first Office Action on the merits that such art has in fact been reviewed. A PTO-1449 or PTO/SB/08 form listing all of the information of record in the prior application is enclosed herewith.

Atty. Docket No.: 4308.4US (99-1199.04/US)

This Information Disclosure Statement is filed within three (3) months of the filing date of the above-identified application, and no certification pursuant to 37 C.F.R. § 1.97(c) or a fee pursuant to 37 C.F.R. 1.17(p) is required.

Respectfully submitted,



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Enclosures: Form PTO-1449 or PTO/SB/08

Document in ProLaw

Form PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION <i>(Use several sheets if necessary)</i>			Docket Number (Optional) 4308.4US (99-1199.04/US)		Application Number Not yet assigned		
			Applicant John T. Moore				
			Filing Date March 2, 2004		Group Art Unit Unknown		
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
	5,567,638	10/1996	Lin et al.				
	5,633,177	05/1997	Anjum				
	6,013,553	01/2000	Wallace et al.				
	6,017,808	01/2000	Wang et al.				
	6,136,654	10/2000	Kraft et al.				
	6,140,024	10/2000	Misium et al.				
	6,251,761	06/2001	Rodder et al.				
	6,261,973	07/2001	Misium et al.				
	6,342,437	01/2002	Moore				
	6,528,396	03/2003	Moore				
FOREIGN PATENT DOCUMENTS							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO
OTHER DOCUMENTS							
(Including Author, Title, Date, Pertinent Pages, Etc.)							
	Al-Shareef et al., "Device Performance of <i>in situ</i> Steam Generated Gate Dielectric Nitrided by Remote Plasma Nitridation", Applied Physics Letters, Volume 78, Number 24, June 11, 2001, pps. 3875-3877.						
	Al-Shareef et al., "Plasma Nitridation of Very Thin Gate Dielectrics", Microelectronic Engineering, 59, 2001, pps 317-322.						
	Hattangady et al., "Ultrathin Nitrogen-Profile Engineered Gate Dielectric Films", IEDM Tech. Dig., 1996, pps. 495-498.						
EXAMINER			DATE CONSIDERED				

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Koh et al., "Plasma-Engineered Si-SiO ₂ Interfaces: Monolayer Nitrogen Atom Incorporation by Low-Temperature Remote Plasma-Assisted Oxidation in N ₂ O", Surface and Coatings Technology, 1998, pps. 1524-1528.
	Lucovsky et al., "Plasma Processed Ultra-Thin SiO ₂ Interfaces for Advanced Silicon NMOS and PMOS Devices: Applications to Si-Oxide/Si Oxynitride, Si-Oxide/Si Nitride and Si-Oxide/Transition Metal Oxide Stacked Gate Dielectrics", Thin Solid Films, 2000, pps. 217-227.
	Mehrotra et al., "A 1.2V, Sub-0.09μm Gate Length CMOS Technology", IEDM Tech. Dig., 1999, pps. 419-422.
	Niimi et al., "Monolayer-Level Controlled Incorporation of Nitrogen in Ultrathin Gate Dielectrics Using Remote Plasma Processing: Formation of Stacked "N-O-N" Gate Dielectrics", J. Vac. Sci. Technology B 17, Nov/Dec 1999, pps. 2610-2621.
	Ting et al., "The Effect of Remote Plasma Nitridation on the Integrity of the Ultrathin Gate Dielectric Films in 0.13 μm CMOS Technology and Beyond", IEEE Electron Device Letters, Vol. 22, No. 7, July 2001, pps. 327-329.

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